## IN THE SPECIFICATION

Please amend the specification as follows:

**The paragraph beginning at page 11, line 4 is amended as follows:**

The foregoing description of blocks 330 and 340 (Figure 3) and Figure 5 correspond to a second phase of a two-phase write cycle in a memory device. In this second phase, transistor ~~406~~ 408 is written with a logical value that is the complement of the logical value written in the first phase. This complementary logical value is written by charging the body of the transistor while not upsetting the charged state of other transistors in the array. Transistor ~~406~~ 408 is part of a single transistor memory cell within an array of memory cells, where the array includes rows and columns. As shown in Figure 5, transistor ~~406~~ 408 is a subset of the transistors in selected row. In some embodiments, the subset includes the entire row of memory cells, such that the second phase of the write charges all of the transistor bodies in the selected row.